## Claims

[c1] What is claimed is:

1.An optical proximity correction (OPC) method for reducing optical proximity effect occurring in a pattern transferring process, the method comprising:

providing a photo-mask;

providing an original photo-mask pattern predetermined to be formed on a surface of the photo-mask, the original pattern comprising at least one integrated circuit layout and at least one blank region;

forming a plurality of dummy patterns in the blank region, the integrated circuit layout, the plurality of dummy patterns, and the residual blank region together composing a corrected photo-mask pattern; and

forming the corrected photo-mask pattern on the surface of the photo-mask;

wherein a phase difference of 180 degrees is detected between a transmitted light of the integrated circuit layout and a transmitted light of the dummy patterns.

[c2] 2.The method of claim 1 wherein the plurality of dummy patterns are used to reduce the difference in pattern density of the original photo-mask pattern so as to modify optical proximity effect occurring in a pattern transferring process.

[c3] 3.The method of claim 1 wherein the plurality of dummy patterns are fabricated around the integrated circuit layout.

[c4] 4.The method of claim 1 wherein the plurality of dummy patterns are fabricated and distributed over the blank region.

[c5] 5. The method of claim 1 wherein the integrated circuit layout is transferred to photoresist layer formed on a surface of a substrate by the pattern transferring process.

[c6] 6.The method of claim 5 wherein the plurality of dummy patterns are nonprintable dummy patterns and not transferred to the photoresist layer during the pattern transferring process.

[c7] 7.The method of claim 6 wherein the dimensions and the numbers of the dummy patterns are designed according to exposure wave length and numerical

apertures of the pattern transferringprocess and the materials included in the photoresist layer.

[c8] 8.The method of claim 7 wherein the edge length of each dummy pattern is a multiple of exposure wave length, and the multiple is less than 0.6.

[c9] 9.The method of claim 7 wherein the distance between each dummy pattern is a multiple of exposure wave length, and the multiple ranges between 0.3 and 2.0.

[c10] 10.The method of claim 7 wherein the least distance between the dummy patterns and the integrated circuit layout is a multiple of exposure wave length, the multiple ranges between 0.4 and 2.0.

[c11] 11.A method of forming patterns on a surface of a photo-mask, the method comprising:
providing a photo-mask; and
forming an integrated circuit layout on the surface of the photo-mask, and forming a plurality of dummy patterns outside the integrated circuit layout on the surface of the photo-mask;
wherein a phase difference of 180 degrees is detected between a transmitted light of the integrated circuit layout and a transmitted light of the dummy patterns.

[c12] 12.The method of claim 11 wherein the plurality of dummy patterns are used to reduce the difference in pattern density on the surface of the photo-mask so as to modify optical proximity effect occurring in a pattern transferring process.

[c13] 13.The method of claim 12 wherein the integrated circuit layout is transferred to a photoresist layer formed on a surface of a substrate by the pattern transferring process.

[c14] 14.The method of claim 12 wherein the plurality of dummy patterns are nonprintable dummy patterns and not transferred to the photoresist layer during the pattern transferring process.

[c15] 15.The method of claim 14 wherein the dimensions and the numbers of the dummy patterns are designed according to exposure wave length and numerical

apertures of the pattern transferring process and the materials included in the photoresist layer.

[c16] 16.The method of claim 15 wherein the edge length of each dummy pattern is a multiple of exposure wave length, and the multiple is less than 0.6.

[c17] 17.The method of claim 15 wherein the distance between each dummy pattern is a multiple of exposure wave length, and the multiple ranges between 0.3 and 2.0.

[c18] 18.The method of claim 15 wherein the least distance between the dummy patterns and the circuit layout is a multiple of exposure wave length, the multiple ranges between 0.4 and 2.0.

[c19] 19.An optical proximity correction (OPC) method for reducing optical proximity effect occurring in a pattern transferring process, the method comprising:
providing a photo-mask;
providing an integratedcircuit layout predetermined to be formed on a surface of the photo-mask;
performing a partial OPC of the integrated circuit layout for obtaining a corrected integrated circuit layout; and
forming the corrected integrated circuit layout on the surface of the photo-mask and forminga plurality of dummy patterns outside the corrected integrated circuit layout on the surface of the photo-mask.

[c20] 20.The method of claim 19 wherein the partial OPC is used to modify pattern transferring defects of the integrated circuit layout comprising right-angled corner rounding, line end shortening, and line width increasing/decreasing.

[c21] 21.The method of claim 19 wherein the plurality of dummy patterns are used to reduce the difference in pattern density on the surface of the photo-mask so as to modify optical proximity effect occurring in a pattern transferring process.

[c22] 22.The method of claim 19 whereinthe plurality of dummy patterns are nonprintable dummy patterns and not transferred to a photoresist layer formed on a surface of a substrate during the pattern transferring process, however, the

integrated circuit layout is transferred to the photoresist layer by the pattern transferring process.

[c23] 23.The method of claim 22 wherein the dimensions and the numbers of the dummy patterns are designed according to exposure wave length and numerical apertures of the pattern transferringprocess and the materials included in the photoresist layer.

[c24] 24.The method of claim 23 wherein the edge length of each dummy pattern is a multiple of exposure wave length, and the multiple is less than 0.6.

[c25] 25.The method of claim 23 whereinthe distance between each dummy pattern is a multiple of exposure wave length, and the multiple ranges between 0.3 and 2.0.

[c26] 26.The method of claim 23 wherein the least distance between the dummy patterns and the integrated circuit layout is a multiple of exposure wave length, the multiple ranges between 0.4 and 2.0.